WHAT IS CLAIMED IS:

1. A method of searching for a pattern in a frame header, the method comprising:

sampling a first set of frame header data;

searching for at least one of a first pattern and a second pattern within a first portion of the first set of frame header data;

upon locating a third pattern within the first portion of the first set of frame header data, shifting the first set of data by one bit;

upon locating a fourth pattern within the first portion of the first set of frame header data, shifting the first set of frame header data by two bits; and

upon locating a fifth pattern within the first portion of the first set of frame header data, shifting the first set of frame header data by three bits, wherein the shifting is performed to align the first set of frame header data to conform with a first standard.

2. The method as defined in Claim 1, further comprising:

examining the shifted first set of frame header data to determine if the shifted first set of frame header data is aligned in conformance with the first standard; and

upon determining that the shifted first set of data is not aligned in conformance with the first standard, generating a shift command.

3. The method as defined in Claim 1, further comprising decoding the shifted first set of data and identifying a first frame byte transition.

4. The method as defined in Claim 1, further comprising performing a run length limited error check on the first set of frame header data, and at least partly in response to determining that an error exists in the first set of frame header data, and synchronizing a receiver clock with a reference clock.

5. The method as defined in Claim 1, wherein the first standard in a SONET standard.

6. The method as defined in Claim 1, wherein the first pattern is "F6" (Hex) and the second pattern is "6F" (Hex).

7. The method as defined in Claim 1, wherein the third pattern is a 11110110 (Binary) at a first location within the first portion.

8. The method as defined in Claim 1, wherein the fourth pattern is a 01101111 (Binary) at a first location within the first portion.

9. The method as defined in Claim 8, wherein the fifth pattern is a 01101111 (Binary) at a second location within the first portion.

10. A framing circuit configured to align frame data, the system comprising:

a memory storage circuit configured to store a sample of frame header data;

a pattern search circuit coupled to the memory storage circuit, the pattern search circuit configured to identify the presence of predetermined patterns in the sample, and, based on the identification, to selectively generate an alignment signal, wherein the alignment signal is used to perform a first alignment of the first sample and the second sample so as to conform with a first standard;

an alignment circuit coupled to the alignment signal and to the memory storage circuit, the alignment circuit configured to shift at least a portion of the sample, to thereby generate a shifted sample in response to the alignment signal indicating that a shift is to be performed;

a third memory storage circuit coupled to the shift circuit, the third memory storage circuit configured to store the shifted sample; and

a byte detect circuit coupled to the third memory storage circuit, the byte detect circuit configured to determine if the shifted sample is misaligned by a first amount, and to generate a second alignment signal in response to determining that the shifted sample is misaligned by the first amount.

11. The framing circuit as defined in Claim 10, wherein the memory storage circuit further comprises a first latch circuit and a second latch circuit, wherein the first latch circuit is configured to store a first part of the sample in response to a first clock pulse, and the second latch circuit is configured to store a second part of the sample in response to a second clock pulse.

12. The framing circuit as defined in Claim 10, further comprising an error detection circuit configured to detect an erroneous pattern in the sample and, upon

detecting an erroneous pattern, generating a synchronization signal indicating that a first clock is to be synchronized with a reference clock.

13. The framing circuit as defined in Claim 10, wherein the first amount is a nibble.

14. The framing circuit as defined in Claim 10, wherein the alignment circuit further comprises a first set of multiplexers and a second set of multiplexers, wherein the first and second sets of multiplexers are independently selectable.

15. The framing circuit as defined in Claim 10, wherein the alignment circuit is configured to shift the portion of the sample by up to three bits.

16. A receiver system configured to search for a pattern in a frame header, the system comprising:

a first memory storage circuit configured to store a first sample of frame header data in response to a first clock signal;

a second memory storage circuit configured to store a second sample of frame header data in response to a second clock signal;

a lock signal configured to cause a receiver clock to be synchronized with a serial bitstream when the lock signal is in a first state, and to cause the receiver clock to be synchronized with a reference clock signal when the lock signal is in a second state;

a run length limited check circuit coupled to the first memory storage circuit and to the lock signal, the run length limited check circuit configured to determine if the first sample contains invalid data and to cause the lock signal to be placed in the second state at least partly in response to determining that the first sample contains invalid data;

a pattern search circuit coupled to the first memory storage circuit, the pattern search circuit configured to search at least a first portion of the first sample for at least a first pattern and a second pattern, and, based on a result of the search, to generate a first plurality of shift signals, wherein the first plurality of shift signals are intended to be used to perform an alignment of the first sample and the second sample so as to conform with a first standard;

a shift circuit coupled to the first plurality of shift signals, the first memory storage circuit, and the second memory storage circuit, the shift circuit configured to shift at least a portion of the first sample and the second sample, to thereby generate a shifted sample, in response to the first plurality of shift signals indicating that a shift is to be performed;

a third memory storage circuit coupled to the shift circuit, the third memory storage circuit configured to store the shifted sample; and

a byte detect circuit coupled to the third memory storage circuit, the byte detect circuit configured to determine if the shifted sample is misaligned by a first amount, and to generate a second shift signal in response to determining that the shifted sample is misaligned by the first amount.

17. The receiver system as defined in Claim 16, wherein the byte detect circuit is further configured to decode the shifted sample and to indicate a first frame byte transition.